What is claimed is:

1. A method of forming a circuit board, comprising the steps of:

a. supplying a non-conducting substrate having a top surface and a bottom surface;

b. forming a plurality of conductive pathways between said top surface and said bottom surface;

c. forming a first circuit pattern on said top surface; and

d. forming a second circuit pattern on said bottom surface.

2. The method of claim 1, further comprising the step of printing one or more circuit devices on said first circuit pattern and on said second circuit pattern.

3. The method of claim 2, wherein said circuit devices are selected from the group consisting of capacitors, inductors, resistors, transformers, and mixtures thereof.

4. The method of claim 3, wherein said first circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of printing a solder mask on said non-solder component of said first circuit pattern and on said circuit devices printed on said first circuit pattern.

5. The method of claim 4, wherein said second circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of printing a solder mask on said non-solder component of said second circuit pattern and on said circuit devices printed on said second circuit pattern.

6. The method of claim 1, wherein said top surface comprises a first conductor and said bottom surface comprises a second conductor, and wherein step b further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas is disposed above one of said plurality of second exposed areas;

removing said first conductor from each of said plurality of first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said top surface and said bottom surface.

7. The method of claim 6, wherein the printing steps further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer

8. The method of claim 7, wherein step c further comprises:

printing a plating resist mask on said top surface to define said first circuit pattern;

plating said top surface increase the thickness of said first circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

9. The method of claim 8, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

10. The method of step 9, wherein step d further comprises:

printing a plating resist mask on said bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

11. The method of step 10, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic

printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

12. A method of forming a multilayer circuit board, comprising the steps of:

a. supplying a first substrate having a first top surface and a first bottom surface;

b. forming a plurality of electrically conductive pathways between said first top surface and said first bottom surface;

c. forming a first circuit pattern on said first top surface;

d. forming a second circuit pattern on said first bottom surface;

e. supplying a second substrate having a second top surface and a second bottom surface;

f. forming a plurality of electrically conductive pathways between said second top surface and said second bottom surface;

g. forming a third circuit pattern on said second top surface;

h. forming a fourth circuit pattern on said second bottom surface;

i. supplying a first insulating layer having a first side and a second side;

j. joining said first side of said first insulating layer to said first bottom surface, and joining said second side of said first insulating layer to said second top surface, such that said first insulating layer electrically insulates said second circuit pattern from said third circuit pattern;

k. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, and said fourth circuit pattern.

13. The method of claim 12, further comprising the step of printing one or more circuit devices on said first circuit pattern, on said second circuit pattern, on said third circuit pattern, and on said fourth circuit pattern.

14. The method of claim 13, wherein said circuit devices are selected from the group consisting of capacitors, inductors, resistors, transformers, and mixtures thereof.

15. The method of claim 12, wherein said first top surface comprises a first conductor and said first bottom surface comprises a second conductor, and wherein step b further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface.

16. The method of claim 15, wherein step c further comprises:

printing a plating resist mask on said first top surface to define said first circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

17. The method of claim 16, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

18. The method of step 17, wherein step d further comprises:

printing a plating resist mask on said first bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

19. The method of step 18, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

20. The method of claim 12, wherein said second top surface comprises a first conductor and said second bottom surface comprises a second conductor, and wherein step f further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said second top surface and said second bottom surface.

21. The method of claim 20, wherein step g further comprises:

printing a plating resist mask on said second top surface to define said third circuit pattern;

plating said second top surface to increase the thickness of said third circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

22. The method of claim 21, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

23. The method of step 22, wherein step h further comprises:

printing a plating resist mask on said second bottom surface to define said fourth circuit pattern;

plating said second bottom surface to increase the thickness of said fourth circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

24. The method of step 23, wherein the printing step further comprises use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

25. The method of claim 12, further comprising the steps of:

l. supplying a third substrate having a third top surface and a third bottom surface;

m. forming a plurality of electrically conductive pathways between said third top surface and said third bottom surface;

n. forming a fifth circuit pattern on said third top surface;

o. forming a sixth circuit pattern on said third bottom surface;

p. supplying a second insulating layer having a first side and a second side;

q. joining said first side of said second insulating layer to said second bottom surface, and joining said second side of said second insulating layer to said third top surface, such that said second insulating layer electrically insulates said fourth circuit pattern from said fifth circuit pattern; and

r. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, said fourth circuit pattern, said fifth circuit pattern, and said sixth circuit pattern.

26. The method of claim 25, wherein said third top surface comprises a first conductor and said third bottom surface comprises a second conductor, and wherein step m further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface.

27. The method of claim 26, wherein step n further comprises:

printing a plating resist mask on said first top surface to define said fifth circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

28. The method of claim 27, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

29. The method of claim 28, wherein step o further comprises:

printing a plating resist mask on said first bottom surface to define said sixth circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

30. The method of claim 29, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

31. A method of forming a circuit board, comprising the steps in sequence of:

a. supplying a non-conducting substrate having a top surface and a bottom surface each covered with a top and a bottom metallic layer, respectively;

b. forming a pattern mask on the top and the bottom metallic layers, leaving exposed metallic patterns;

c. building-up the exposed metallic patterns to increase the thickness thereof;

d. removing the pattern mask whereby to expose the metallic patterns; and

e. etching the metallic layer coated substrate from step d whereby to remove exposed metallic surfaces, while leaving intact at least a portion of the built-up metallic patterns.

32. The method of claim 31, wherein said pattern mask is applied by printing.

33. The method of claim 32, wherein said printing comprises electro-photographic printing, ink jet printing, release press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

34. The method of claim 33, wherein said printing is effected employing a fusable ink.

35. The method of claim 34, wherein said fusble ink comprises a polymeric binder ink containing colloidal metal.

36. The method of claim 35, wherein the colloidal metal comprises colloidal silver or colloidal palladium.

37. The method of claim 32, including the step of pre-heating the substrate prior to printing.

38. The method of claim 37, where the board is preheated to a temperature in the range of 100°C-160°C.

39. The method of claim 31, wherein said exposed metallic patterns are built-up by plating.

40. The method of claim 12, and further comprising the step of removing the resulting multiplayer circuit board from the first substrate.